Roll No. .....

22670

M. Tech. 2nd Semester CBCS Scheme Examination – May, 2018

VLSI DESIGN

Paper : MTECE22D4

Time : Three Hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt any ***five*** questions in all. Question No. **1** is ***compulsory*** selecting any ***one*** question from each Section. All questions carry equal marks.

1. Explain the following :

(a) MOS Transistor 5

(b) Channel Length Modulation 5

(c) Drain Punch-Through 5

(d) Scaling Factors 5

SECTION – A

2. (a) What is the meaning of enhancement and depletion in MOSFET ? Discuss in brief the theory of enhancement type MOSFET with suitable diagrams used. 10

(b) What is the difference between N-MOS and P-MOS ? Which one is preferred over the other ? Explain in detail. 10

3. Explain in brief the CMOS fabrication using : 20

(i) P-well Process

(ii) N-well Process

SECTION– B

4. In the inverter circuit, what is meant by $Z_{p.u.}$ and $Z_{p.d}$? Derive the required ratio between $Z_{p.u.}$ and z.d if an n-MOS inverter is to be driven from one or more Pass Transistors. 20

5. (a) What do you mean by Latch-up problem in CMOS circuit ? How can it be avoided ? Explain . 10

(b) What do you mean by VTC in CMOS Inverter ? Explain it along with the working of the CMOS inverter in detail. 10

SECTION – C

6. What do you mean by the following :

(i) Delay unit and inverter delay. 5

(ii) Propagation Delay. 5

(iii) Supper Buffers 5

(iv) Double metal Single Poly Silicon 5

7. Draw stick diagram of the given equations :

(i) Y= A.B.C+D.E.F 7

(ii) 2-input NOR Gate 7

(iii) CMOS Inverter 6

SECTION – D

8. What is the meaning of Scaling of MOS transistors ? What are the different factors used in scaling ? Explain. Also discuss about the limitations of the scaling. 20

9. Explain the following :

(i) Design of ALU Subsystem 5

(ii) Carry Look ahead Adder 5

(iii) PLA 5

(iv) Switch Logic and Gate Logic 5