22151

M.Tech. 2nd Semester (ECE) Examination, May–2017

VLSI DESIGN

Paper–MEEC-506

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt any **five** questions. All questions carry equal marks.*

1. (a) Draw and explain the basic MOS transistor structure in depletion mode along with its symbol and V-I characteristics. 10

(b) Compare and contrast CMOS and Bipolar Technology. 10

2. (a) Explain the CMOS inverter working and sum up its DC characteristics in all operataing regions. 10

(b) Explain the steps involved in the fabrication of N-well CMOS. 10

3. (a) Write in detail about various MOS capacitances. 6

(b) Draw latch up on CMOS circuits. 6

(c) Realize all gates with the help of PMOS technology. 8

4. (a) Design a positive edge triggered D-register. 6

   (b) Explain the different steps of twin tub CMOS fabrication process with neat diagram. 14

5. (a) Write the steps involved in CMOS design style using stick diagrams. Design it for NAND gate. 10

   (b) Explain the Lambda Based design rules for digital air circuits. 10

6. (a) Realize the function using CMOS. 10

   $$Y = \overline{x}_1 + |\overline{x}_2 + \overline{x}_3|\overline{x}_4$$

   (b) How we can insert propagation delay in a circuit ? Explain various ways for it. 10

7. Explain all the scaling factors for device parameters. Derive values for all the parameters.

8. Write short note on :

   (a) ATPG methods

   (b) Design and testability

   (c) Long simulation design validation

   (d) Design of ALU using CMOS. 20