**M. E. 2nd Semester ECE Examination, May–2015**

**VLSI DESIGN**

**Paper–MEEC-506**

*Time allowed : 3 hours]* *[Maximum marks : 100*

***Note :*** *Attempt any five questions. All questions carry equal marks.*

**1.** (a) Discuss in brief theory of Depletion type MOSFET.

(b) Discuss in brief the fabrication of CMOS using N-well process. 10

**2.** Explain the following :

(a) Body effect

(b) Channel length modulation

(c) Pass transistor. 20

**3.** (a) Discuss the MOS transistor circuit model. 10

(b) What is transistor sizing ? Explain with examples. 10

**4.** (a) Discuss the CMOS design rules and importance of power and delay in the logic design. 10

(b) Draw the stick diagrams for :

(i) Two I/P CMOS NOR gate

(ii) CMOS Inverter. 10

5. Discuss in brief the constant field scaling and constant voltage scaling. Also discuss the scaling of inter connects and scaling limitations. 20

6. (a) Discuss in brief the Pseudo-NMOS invertor. 10

(b) Discuss the clocked sequential circuits with examples. 10

7. (a) Design a carry look ahead adder optimized for speed, cycle operation and layout. 10

(b) Discuss in brief the super buffers. 10

8. Write short notes on :

(a) Domino logic circuit

(b) Propagation delay

(c) Architecural issues in VLSI. 20