Roll No. .....

22148

M.E. IInd Semester (E.C.E.)

Examination–May, 2014

ELECTRONICS SYSTEM DESIGN

Paper- MEEC-502

Time : 3 hours ***Max. Marks : 100***

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard will be entertained after the examination.

Note : Attempt any **five** questions.

1. (a) Explain XOR and AND-OR Inverter Gates. *10*

(b) Explain Tri-state Bus system. *10*

2. (a) Explain clocked JK Flip-Flop *10*

(b) Explain D flip flop *10*

3. (a) Discuss CPLD and FPGA in detail. *10*

(b) Explain PLA and PAL based design. *10*

4. (a) Explain Multiplexers in system controller. *10*

(b) What is Indirect Addressing in multiplexers configuration ? *10*

5. (a) Design steps for next state Decoders. *10*

(b) Explain Ring counter using serial shift register. *10*

6. Write short notes on: 20

(a) Design of asynchronous machines.

(b) MEV Approaches to Asynchronous Design.

7. Explain any **two** : 20

(a) Propagation delay

(b) MSI decoders

(c) Arithmetic circuits

8. Explain controller design phase to system documentation. 20
