Roll No. .....

67043

M.C.A. 1st Sem. w.e.f. Dec. 2012 with New Notes (Current Scheme)

Examination–December, 2014

Digital Design

Paper-MCA-103

Time : 3 hours ***Max. Marks : 80***

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard will be entertained after the examination.

Note : Question No. **1** is **compulsory**. Attempt **four** more questions selecting **one** question from each unit.

8 × 2 = 16

1. (a) Convert $(A72E)_{16} = (\ )_8$

(b) Prove $A \oplus B = \overline{A} \oplus \overline{B}$

(c) Draw circuit diagram for CMOS NAND gate.

(d) Convert $Y = AB + A\overline{C} + BC$ into standard SOP form.

(e) Write the advantages of PLA.

(f) What is race round condition ?

(g) Differentiate between SRAM and DRAM.

(h) Realize using EXOR gate $Y = A \oplus B \oplus C \oplus D$

Unit-I

2. (a) Perform the following conversions : *4*

$(39.12)_{10} = (\ )_2$

$(268)_{10} = (\ )_{16}$

(b) Calculate the following : *12*

(i) 1011×100 (ii) 11011×1001

(iii) $1000 \div 10$ (iv) $101010 \div 111$

(v) $(23)_8 + (67)_8 = (\ )_2$

(vi) $(37)_8 - (53)_8 = (\ )_8$

3. (a) Explain the concept of parity bits with reference to even detection. *8*

(b) Construct hamming code for BCD 0110. Use even parity. *4*

(c) Discuss how floating point numbers can be represented ? *4*

Unit-II

4. (a) Draw logic circuit for the given identity. *4*

(i) $X = \overline{AB + C} + \overline{BC}$

(ii) $4 = \overline{AB + C} + B\overline{C}$

(b) What is propagation delay. *4*

(c) Simply the functions using K map *8*

(i) $X = \overline{A}\,\overline{D} + A\,\overline{B}\,\overline{D} + \overline{A}\,\overline{C}\,D + \overline{A}\,CD$

(i) $f(W,X,Y,Z) = \sum(0,1,2,3,4,7,8,11,12,14,15)$

5. (a) Explain the working of CMOS inverter. *6*

(b) Simplify the Boolean expression.

5×2=10

(i) $F = A\overline{B}\,C\left(\overline{\overline{A}\,\overline{B} + AB\overline{C}\,D}\right)$

(ii) $F = \overline{A}\,\overline{B}\,C + B\overline{C} + \overline{A}BC + ABC$

Unit-III

6. (a) Design a 1 bit comparator which can compare A = B, A > B, A < B. *8*

(b) Shaw the D flip flop implementation from JK flip flop. 4

(c) What are different forms of triggering in flip flops ? Discuss. 4

7. (a) Explain the working of full subtractor. 8

(b) Design a combinational circuit using a ROM that accepts a 2-bit number and generates on output binary number equal to the square of the input number. 8

Unit-IV

8. (a) Design a synchronous mod-6 counter using JK flip-flop. 10

(b) Explain the operation of 4-bit universal shift register. 6

9. (a) Why SRAM is faster than DRAM ? Discuss. 6

(b) Explain the operation of 4-bit SIPO shift register. 10