

Roll No.

24043

**B. Tech 3rd Semester (IT)
Examination – December, 2017**

DIGITAL ELECTRONICS

Paper : EE-204-F

Time : Three Hours]

[Maximum Marks : 100

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note: Attempt five questions, Question No. 1 is compulsory and one question from each Sections. All questions carry equal marks.

1. (a) What is Latch ? 5 × 4 = 20
- (b) Realize EX-OR gate using NAND gate.
- (c) Differentiate :
Ripple counter and synchronous counter.
- (d) Draw and explain circuit for one bit comparator.

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P. T. O.

SECTION - A

2. (i) Multiply $(5.65)_8$ by $(2.432)_8$ 20
(ii) Divide $(50.1)_8$ by $(3)_8$
(iii) Convert $(ABD73)_{16}$ into $()_8$
(iv) Convert $(34674)_8$ into $()_2$
(v) Subtract $8 - 10$ using 2's compliment.
3. (a) What are universal gates ? Derive basic gates from universal gates. 10
(b) Design the ckt. after minimizing using k-map 10
 $f(A, B, C, D) = \sum(0, 1, 2, 3, 6, 7, 9, 13) + \sum(11, 15)$

SECTION - B

4. (a) Explain full adder with truth table and circuit. 10
(b) Explain 3-8 decoder. 10
5. (a) Design BCD to 7 segment decoder. 10

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- (b) Seven bit hamming code is received as 1011001 locate the error position and find the correct code, if even parity is used. 10

SECTION - C

6. (a) What is race round condition and how we can remove it? 10
(b) Explain bidirectional shift register. 10
7. (a) Construct D-flip flop using JK-flip flop. 10
(b) Explain 4 bit comparator. 10

SECTION - D

8. (a) Design the circuit of half adder using ROM. 10
(b) Explain TTL. 10
9. Write short notes on : 20
(a) PLD's and CPLD's
(b) PAL and PLA

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