24043

B.Tech. 3rd Semester (I.T.) Examination,
December–2016

DIGITAL ELECTRONICS

Paper–EE–204–F

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *The candidate will be required to attempt **five** questions in all at least **one** question from each unit.*

Question No. 1 is compulsory.

1.	(a)	What is meant by parity bit ?	1
	(b)	Define duality property.	1
	(c)	State De Morgan's theorem.	2
	(d)	What is encoders and decoders ?	4
	(e)	Define sequential circuits and latches.	2
	(f)	Difference between latches and flip flop.	2
	(g)	What is the difference between PLA and PAL ?	2
	(h)	What is the asynchronous sequential logic ?	2
	(i)	Explain hamming codes with example.	2
	(j)	Define binary codes, cyclic codes, error detecting and error correcting codes.	2

Unit–I

2. (a) Design a simple logic circuit such that the output is 1 when the binary numbers A, B, C, D is greater than 0110. 8

(b) In a 4-input NAND gate, two inputs are to be used. What are the options available for the unused inputs and which one is the best and why ? 7

(c) What is prime implicants ? and state distributive law. 5

3. (a) Perform the following operations on the given binary numbers a specified :

(i) 110.01 + 1.011 1

(ii) Convert 11101.01 to decimal 1

(iii) 11100.101–101.01 using 2's compliment. 1

(iv) State whether the following statement is true or false :

"All decimal fractions have exact binary equivalents" and justify your answer. 2

(b) Solve the following expression by mapping :

$F = \Sigma m (0, 2, 3, 6, 7, 8, 9, 10, 13)$.

Write the steps involved in solving this Quine-McClusky method. 7

(c) Perform the operation $(12_{10} - 35_{10})$ using 2's compliment method. 2

(d) Obtain the minimal SOP expression for

$Y (A, B, C, D) = \in m (2, 3, 5, 7, 8, 9, 11, 12, 13, 14, 15) + d (2, 4)$ using k-map. Realize the expression using 2-input NAND gates only. 6

Unit–II

4. (a) Construct a 4-input multiplexer using four 3-input AND gates, an OR gate and three inverters. Show the input, output and select lines and write a table showing the outputs for various select inputs. 8

(b) Design a combinational circuit that accepts a 3-bit number as input and generates an output binary number equal to square of the input number. 5