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**B. Tech. 6th Semester (Electronics and Communication
Engineering) Examination, May-2013**

VLSI DESIGN

Paper-EE-306-F

Time allowed : 3 hours] [Maximum marks : 100

Note : Question number 1 is compulsory and attempt one question from each of the four sections. All questions carry equal marks.

1. (a) What are the disadvantages of BiCMOS transistor over MOSFET transistor ? 3
- (b) Why AOI implementation is better than NAND-NAND and NOR-NOR implementation ? 4
- (c) Briefly explain different steps involved in the fabrication of an integrated circuit. 5
- (d) What do you mean by tally circuits ? 4
- (e) Write down a program in VHDL language for AND Gate. 4

Section-A

2. (a) Describe various steps involved, with the help of a neat and clean diagram, in the fabrication of a NMOS. 10
- (b) Deduce the current voltage relationship for NMOS transistor. 10

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3. (a) What are the different parameters affecting the working of MOSFET at high frequency ? Explain your answer with the help of high frequency model of MOSFET. 10
- (b) What do you mean by latch-up in CMOS ? What are the remedies for the latch-up problem in CMOS ? 10

Section-B

4. (a) Explain the DC characteristics of CMOS inverter. 10
- (b) What do you mean by Design Rules and layout? Also explain Lambda based design rules. 10
5. (a) Derive an expression for Pull-up to pull down ratio for NMOS inverter driven through one or more pass transistor. 10
- (b) Draw a neat and clean stick diagram and physical layout for CMOS 2-input NAND gate. 10

Section-C

6. (a) Realise following functions using CMOS logic gate circuits.
- (i) $Y = (A+B)(C+D)$ (ii) $Y = (AB+CD)$

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- (b) With the help of neat and clean diagram explain the implementation of a 4-bit barrel shifter. 10
7. (a) With the help of a neat and clean Stick diagram and layout, explain the working of Static CMOS latch. 10
- (b) Compare the NAND-NAND and NOR-NOR circuit implementation design. 10

Section-D

8. (a) Explain the different programmable logic Devices. 10
- (b) Explain different modeling styles of specifying architecture body of an entity in VHDL. 10
- (c) Explain Mealy and Moore Machine. 10
- (d) Explain different Subprograms present in VGDL. 10