B.E. 4th Semester (ECE) Examination,

May–2013

DIGITAL ELECTRONICS

Paper–EE–204-E

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt any **five** questions.*

1. (a) A 7-bit hamming code is received as 1010110, in which at most a single error has occurred. Locate the position of the error using even parity being used. 10

   (b) Explain following :

   (i) r's compliment

   (ii) (r–1)'s compliment. 10

2. (a) What is the limitation of k-map method ? Explain Quine-McClusky method of minimization. 10

   (b) Obtain minimal POS and SOP expressions for :

   $Y(A, B, C, D) = \Sigma (0, 1, 4, 5, 9, 11, 13, 15)$ 10

3. (a) Draw the circuit of a two-bit magnitude comparator and explain its operation. 10

   (b) Design a circuit to realize :

   $Y = X W \overline{Z} + X Z \overline{W} + \overline{X} W Z + X ZW$ 10

4. (a) Explain that a D-flip flop can commonly be used as a delay switch. 10

   (b) Implement mod-8 binary counter using SR flip-flops. 10

5. (a) What is tri state logic ? Why it is constructed ? How many output states are exhibited by a three state gate ? 10

   (b) Draw the circuit of a two input TTL NAND gate. Explain its operation. What is totempole output ? 10

6. (a) Draw and explain the operation of a 8-bit successive approximation ADC. What is the maximum conversion time for this ADC ? 10

   (b) Draw the sample and hold circuit and explain. 10

7. (a) Differentiate between : 10

(i) Fixed logic and programmable logic.

(ii) PAL and PLA devices.

(b) Explain the internal architecture of a PLA. 10

8. Write notes on :

(i) CPLD

(ii) Interfacing of CMOS and TTL families.

(iii) Display devices. 7+7+6