**B.Tech. 7th Semester (F) Scheme (CSE)**

**Examination, December–2018**

**ADVANCED COMPUTER ARCHITECTURE**

**Paper– CSE–401–F**

*Time allowed : 3 hours]* *[Maximum marks : 100*

***Note: Question No. 1 is compulsory.*** *Attempt **five** questions in total, selecting **one** question from each Section.*

1. (a) Define command and machine. 5×4=20

   (b) Does n-segment pipelining increases speed by n time? Justify your answer.

   (c) Compare Cold and Warm Caches.

   (d) Define Memory Bank and Memory Module.

   (e) What do you mean by clustering?

**Section–A**

2. (a) What is cycle quantization? Find the effect of cycle quantization on Pipelining. 10

   (b) Describe Virtual to Real mapping method. 10

or

3. (a) Differentiate between hard wired control and micro programmed control. 10

   (b) Explain various kinds of overhead in pipeline processing. 10

**Section–B**

4. (a) What are two strategies for memory updation on a write in cache? Describe. 10

(b) How to overlap T–Cycle in V–R Translation? 10

or

5. (a) Describe Level Caches and Sectored Caches in detail. 10

(b) Describe Set- associative mapping scheme for Cache memory. 10

## Section–C

6. Describe Rau's Strecker's and Hellerman's memory model in detail. 20

or

7. Explain mixed Queen Model and Delta Binomial model in detail. 20

## Section–D

8. (a) What is Vector Memory? What are vector instructions / operations? 10

(b) Compare vector processors and multiple Issue Machines. 10

or

9. (a) Write note on "Memory Coherency in Shared multiprocessors. 10

(b) What is the effect of grain size on the amount of parallelism in multiprocessor system? 10