

24487

B.Tech. 7th Semester (CSE)  
Examination, December-2015

**ADVANCED COMPUTER ARCHITECTURE**

**Paper-CSE-401-F**

*Time allowed : 3 hours*                      *[Maximum marks : 100]*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after the examination.

*Note : Attempt five questions. Question No. 1 is compulsory. Select one question from each section.*

1. (a) What are the basic data type ? Explain briefly.
- (b) What is Split-I and D-caches ?
- (c) What is memory Module ?
- (d) What is vector processor ?
- (e) What is two level cache ?

**Section-A**

2. (a) Assume a wafer has diameter of 21 cm and costs 5000 for a particular production run. Compute the cost per die for die area =  $2.3 \text{ cm}^2$  and for  $1 \text{ cm}^2$  if  $p_D = 1 \text{ defect/cm}^2$ .
- (b) Explain processor evaluation matrix.

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3. (a) Explain basic instruction timing with example.
- (b) What is Virtual to Real mapping ? Explain.

#### Section-B

4. (a) Explain various cache write policies.
- (b) Explain strategies for line replacement at miss time.
5. (a) We have two level cache with miss rate of 4%(L1) and 1%(L2). Suppose the miss in L1 and Hit in L2 penalty is 2 cycle, and the miss penalty in both caches is 7 cycle(5cycle more than a hit in L2). If a processor makes 1.5 reference instruction, compute the excess CPI due to cache miss.
- (b) What are three general approach to avoiding the serial translation step in cache access.

#### Section-C

6. Describe memory modeling using queuing theory. Explain closed queues model in detail.
7. (a) What are the various step in the design of the memory system ? Explain.
- (b) Describe Hellerman's and Rau's model in detail.

#### Section-D

8. (a) Compare Vector and Multiple-Issue Processors
- (b) What are the issue which effect the performance of a vector processor.
9. (a) Discuss partitioning in multiprocessor.
- (b) What are the different type of shared memory multiprocessors ? Explain.