7. Explain the following:

(a) Magnetic Disks [8]

(b) Characteristics of Memory Cell [8]

UNIT-IV

8. (a) What are Interrupts ? How are these useful ? What is Interrupt structure ? Illustrate. [8]

(b) What are I/O Channels ? How do these work ? Illustrate their working. [8]

9. Explain the following:

(a) Instruction Format [8]

(b) Instruction Cycle [8]

Roll No. .....

97666

B.C.A. 2nd Semester Examination–May, 2017

Logical Organisation of Computers

Paper-BCA-107

Time : 3 hours ***Max. Marks : 80***

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard will be entertained after the examination.

Note : Attempt **five** questions in all. Question No.1 is **compulsory** and attempt **four** more questions by selecting **one** question from each unit. All questions carry equal marks.

1. Compulsory questions [8×2]

(a) What is clocked RS flip-flop ?

(b) Why Master-Slave flip-flop is called so ?

(c) What is up-down counter ?

(d) What is an Instruction Format ?

(e) What are applications of ROM ?

(f) What is a program-controlled I/O technique ?

(g) What is an IOP ? State its significance.

(h) What characterizes Flash Memory ?

UNIT-I

2. (a) What are Excitation Tables ? How are these relevant ? Draw Excitation Table for RS and JK flip-flop. [8]

(b) What are State Diagrams ? How are these relevant in design of Flip-flops ? Explain. [8]

3. Explain the following:

(a) Master-Slave Flip-Flop [8]

(b) T Flip-flop [8]

UNIT-II

4. (a) What are Synchronous Binary Counters ? Draw its block diagram and illustrate its operation. [8]

(b) What are the general characteristics of good shift registers ? Design a 4-bit shift register and outline the procedure for serial to parallel conversion and vice-versa. [8]

5. Explain the following:

(a) Asynchronous Sequential Circuit [8]

(b) Modulo-5 Counter [8]

UNIT-III

6. (a) What are I/O Device Controllers ? How do these work ? Illustrate their working. [8]

(b) What is Semiconductor RAM ? How do you design a RAM cell ? Illustrate. [8]